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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/790,492 | 03/01/2004 | Lingyi A. Zheng | MIO 0082 N2/40509.292 | 9512 |

23368 7590 03/21/2007

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| EXAMINER | |
|---|---|
| THOMAS, TONIAE M | |
| ART UNIT | PAPER NUMBER |
| 2822 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/21/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/790,492 | ZHENG ET AL. | |
| | Examiner | Art Unit | |
| | Toniae M. Thomas | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 January 2007 has been entered.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 5,905,280) in view of Lee et al. (US 2002/0068466 A1) and Schuegraf et al. (US 5,624,865).[1]

Lin et al. (referred to hereinafter as Lin) discloses a process for forming a memory cell (figs. 1-8, 10 and accompanying text). The process comprises: forming a semiconductor structure defining a transistor 18 and a pair of

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[1] Both the Lee et al. and Schuegraf et al. references have been relied on in previous Office actions. Applicant submitted the Lin et al. reference as prior art (see 1449 filed on 06 June 2004). However, the Lin et al. reference has not been relied on prior to this action.

transistor node locations 22, 24 in a semiconductor substrate 12 (fig. 1 and col. 3, lines 3-22); forming a BPSG insulating layer 28 over the substrate (fig. 2 and col. 3,lines 31-36); forming a container in the insulating layer over one of the node locations (fig. 6 and col. 4, lines 25-29); forming an HSG polysilicon lower electrode layer 46 along an inner surface of the container, wherein the HSG polysilicon lower electrode layer is formed so as to extend beyond the inner surface of the container, and the HSG polysilicon lower electrode layer defines a lateral portion which extends at least partially along the upper surface of the insulating layer (figs. 7, 8 and col. 4, lines 54-66); forming a silicon nitride dielectric layer 54 over the HSG layer and an upper surface of the insulating layer (fig. 8 and col. 5, lines 34-36); and forming an upper electrode layer (fig. 8 and col. 5, lines 36-38).

Lin lacks anticipation of forming the silicon nitride layer to a thickness of less than 50 angstroms using an atomic layer deposition process, and forming a reoxidized layer over the silicon nitride layer.

The Lee et al. application publication (referred to hereinafter as Lee) is relied upon in this rejection because the reference teaches forming a silicon nitride dielectric layer through an ALD process (see figs. 2A-2F and accompanying text). Lee discloses an ALD method for depositing a silicon nitride layer, wherein after loading a semiconductor substrate into a reaction chamber (par. 25, lines 4-9), a silicon-containing precursor is chemisorbed over a surface of the substrate (fig. 2A and par. 25, lines 9-13), and then a nitrogen-

containing precursor is reacted with the chemisorbed silicon-containing precursor to form a silicon nitride dielectric layer (fig. 2E and par. 27, lines 1-6). The silicon nitride layer to a thickness of 2 angstroms, which is significantly less than the required thickness of "less than about 50 angstroms (par. 0028, lines 4-7).

The Schuegraf et al. patent (referred to hereinafter as Schuegraf) is relied on this rejection because the reference teaches the claimed step of depositing a reoxidized layer over a silicon nitride dielectric layer. In a process similar to that of Lin, Schuegraf discloses the steps of: forming an HSG polysilicon lower electrode layer 58 along an inner surface of the container 54, wherein the container is formed in an insulating layer 50 which may comprise BPSG (figs. 6, 7 and col. 5, lines 40-52); forming a silicon nitride dielectric layer 64 over the HSG layer and an upper surface of the insulating layer (fig. 8 and col. 5, lines 7-11); forming a reoxidized layer 68 on the silicon nitride layer (fig. 9 and col. 6, lines 26-28); and forming an upper electrode layer 72 on the reoxidized layer (fig. 9 and col. 6, lines 22-28).

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify Lin by (1) forming the silicon nitride dielectric layer using an atomic layer deposition process and (2) forming a reoxidized layer on the silicon nitride layer, as taught by Lee and Schuegraf, respectively, because: (1) as compared with conventional chemical vapor deposition (CVD) methods, for example low-pressure chemical vapor deposition

(LPCVD), a silicon nitride film deposited using an ALD process has excellent step coverage and uniformity (Lee - par. 3, line 8 - par. 5, line 7) and, therefore, will uniformly conform to the uneven topography of the underlying HSG layer; and (2) forming a reoxidized layer on the silicon nitride dielectric layer reduces leakage current of the silicon nitride layer, and provides generally acceptable storage properties (col. 2, line 63 - col. 3, line 5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T. M. Thomas

Toniae M. Thomas
Patent Examiner
Technology Center 2800

TMT
20 January 2007